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GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/862,471	KAWAGUCHI, MITSUHARU	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004 and 02 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

Papers Received

2. Receipt is acknowledged of the amendment papers where the papers have been placed of record in the file.

3. The objections to the specification, drawings, and claims as well as the 35 USC 112 rejections have been overcome by the amendment and are withdrawn. New objections to the drawings and new 35 USC 112 rejections have been added as given below.

Drawings

4. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the new drawings are not labeled "Replacement Sheet". Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. Further, a review from the Draftsperson, with their objections listed, is attached. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

5. Claim 10 objected to because of the following informalities: line three should read "group are operation".

6. Claim 11 objected to because of the following informalities: The preamble of the claim is somewhat unclear because the buffer queue control is made up of what appears to be the substance of the buffer itself.

7. Claim 11 is objected to because of the following informalities: the preamble refers to the physical structure of a control circuit when lines 12-20 are regarding steps of this circuit. The claim is of improper dependent form for incompatible statutory subject matter. A control circuit cannot comprise steps nor can a claim explicitly contain both structural and method limitations.

8. Claim 11 is objected to because of the following informalities: there are many grammatical errors throughout the claim. These include (with emphasis):

a. In lines 3-4 "instruction" should read "instructions" and should be followed by a semicolon (;) rather than a colon (:).

b. In line 7, "instruction" should read "instructions"

c. Line 9 should read "after said first instructions;"

d. Line 11 should read "order of instructions"

e. Line 14 should read "instruction that is issued"

f. Line 18 should read "instructions"

g. Line 20 should read "instructions" twice

These are just examples and similar errors exist in the dependent claims as well and must be corrected. Appropriate correction is required.

9. Claim 12 is objected to because of the following informalities: body of the claim is discussing a method step and the preamble refers to a control circuit. The claim is of improper dependent form for incompatible statutory subject matter.

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claims 1-4 and 6-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

12. buffer - comp sci: an area used to store data temporarily

13. The language of claims 1-4 raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment, or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 USC 101. Claims 1-4 simply describe an instruction buffer that is not necessarily tangibly bodied. Each of the limitations can be interpreted as mental steps or ideas that can be drawn by pencil and paper. The specification gives no specific definition of "buffer" but merely uses buffers. The included dictionary definition of "buffer" as it relates to computer science (which is the art defined in the specification) states an "area used to store data temporarily". One can easily draw such an area or box on paper and store data such as sequences of instructions with entry numbers.

14. The language of claims 6-10 raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment, or

machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 USC 101. Claims 6-10 simply describe a method of controlling a buffer queue that is not necessarily tangibly bodied. Each of the limitations can be interpreted as mental steps that can be drawn by pencil and paper. For example, one can easily generate groups of instructions in a certain order by writing them on paper. One can then draw out the execution of an instruction and the results it provides.

15. The language of claims 11-15 raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment, or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 USC 101. Claims 11-15 simply describe an instruction buffer that is not necessarily tangibly bodied. Each of the limitations can be interpreted as mental steps or ideas that can be drawn by pencil and paper. The specification gives no specific definition of "buffer" but merely uses buffers. The included dictionary definition of "buffer" as it relates to computer science (which is the art defined in the specification) states an "area used to store data temporarily". One can easily draw control for such an area or box on paper that stores data such as sequences of instructions that are shifted, released, deleted, or issued to another location.

Claim Rejections - 35 USC § 112

16. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

17. Claims 1-4 and 11-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

18. The term "relatively lower entry number" in claim 1 is a relative term which renders the claim indefinite. The term "relatively lower entry number" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It cannot be determined with certainty what the entry number is lower than. The Examiner is taking the claim to mean, "relatively lower entry number than another instruction in another entry," as implied by the claims.

19. The term "relatively higher entry number" in claim 1 is a relative term which renders the claim indefinite. The term "relatively higher entry number" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It cannot be determined with certainty what the entry number is higher than. The Examiner is taking the claim to mean, "relatively higher entry number than said one instruction of said sequence of instructions," as implied by the claims.

20. Claim 1 recites the limitation "the entries" in line 9. There is insufficient antecedent basis for this limitation in the claim. Two buffers with entries have been defined in the claim and it cannot be ascertained which is spoken of. The Examiner is taking the claim to mean "the entries of the first buffer".

21. Claim 1 recites the limitation "another entry" in line 10. There is insufficient antecedent basis for this limitation in the claim. Two buffers with entries have been defined in the claim and it cannot be ascertained if this entry is another entry of either of the two buffers or possibly a separate entry in a different buffer. The Examiner is taking the claim to mean "an entry of the first buffer different from the entry containing the one instruction" as implied by the claim language.

22. Claim 2 recites the limitation "the entries" in line 1. There is insufficient antecedent basis for this limitation in the claim. Two buffers with entries have been defined in the claims and it cannot be ascertained which is spoken of. The Examiner is taking the claim to mean "the entries of the first buffer".

23. Claim 3 recites the limitation "the entries" in line 2. There is insufficient antecedent basis for this limitation in the claim. Two buffers with entries have been defined in the claims and it cannot be ascertained which is spoken of. The Examiner is taking the claim to mean "the entries of the first buffer".

24. Claim 3 recites the limitation "said entries" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. Two buffers with entries have been defined in the claims and it cannot be ascertained which is spoken of. The Examiner is taking the claim to mean "said entries of the first buffer".

25. Claim 4 recites the limitation "the entries" in line 1. There is insufficient antecedent basis for this limitation in the claim. Two buffers with entries have been defined in the claims and it cannot be ascertained which is spoken of. The Examiner is taking the claim to mean "the entries of the first buffer".

26. Claim 3 recites the limitation "the entries" in line 2. There is insufficient antecedent basis for this limitation in the claim. Two buffers with entries have been defined in the claims and it cannot be ascertained which is spoken of. The Examiner is taking the claim to mean "the entries of the first buffer".

27. In claim 11 the phrase "a reorder buffer for subsequently registering a plurality of instructions" is very unclear. It cannot be determined what the function is subsequent to. The Examiner is interpreting the claim with the word "subsequently" omitted.

Claim Rejections - 35 USC § 102

28. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

29. Claims 1-4 and 6-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Rupley (6,157,998).

30. In regard to claim 1, Rupley discloses an instruction buffer comprising:

a. a sequence of instructions arranged in an order determined beforehand; a first buffer including entries arranged in a preselected entry number order for storing said sequence of instructions; [Column 6, lines 28-31 show that a group, or sequence, of instructions are stored in an instruction buffer in program order (an order determined beforehand). Figures 2-10 show this buffer (element 20)

and that it has separate entries with entry numbers (and thus the instructions are in an entry number order) for storing the instructions.]

b. a second buffer including other entries for storing instructions, wherein an instruction stored in any one of said other entries earlier than other instructions is issued earlier than said other instructions. [Figures 2-10 show that there is a second buffer 28a-c. Column 3, lines 34-52 illustrate that these buffers include age bits for specifying what instructions in the buffers are earlier than the other instructions in the buffers. Column 7, lines 24-27 further show this. The progression given in figures 4-7 shows that instruction ("an instruction" of the claim) BC_0 is stored in buffer 28 earlier than other instructions BC_1 and BC_2 are stored in this buffer. These figures will also show that the BC_0 instruction is also issued or dispatched (removed from the instruction buffer and placed in the completion buffer) before the other instructions.]

c. wherein any one of said sequence of instructions stored in any one of the entries designated by a relatively lower entry number is prior, in order, to another instruction stored in another entry designated by a relatively higher entry number. [Figures 4-10 illustrate a progression of the sequence of instructions through the buffer. The figures show that each buffer entry is designated by an entry number ranging from 0 to 7. The progression given in figures 4-5 show specifically that an instruction with a lower entry number (0) is dispatched from the instruction buffer before, and is thus prior in order to, an instruction with a higher entry number such as the instruction at entry 7.]

31. In regard to claim 2, Rupley discloses the instruction buffer as claimed in claim 1, wherein the entries each show whether or not the instruction stored therein is ready to be issued. [Column 7, lines 59-67 show that the buffer is first-in-first-out (FIFO) in nature and after dispatch, or issue, of an instruction each instruction in the buffer decrements down into an entry with a lower entry number. Thus, as shown in figures 4-5, the instruction at entry 0 is ready to be issued. This is shown by the entries based on the entry number and if it is 0 or not.]

32. In regard to claim 3, Rupley discloses the instruction buffer as claimed in claim 2, wherein the instruction is first issued from, among the entries whose instructions are ready to be issued, the entry having a lowest entry number. [As shown above, the instruction first issued from is at entry 0 and thus at the entry with the lowest number.]

33. In regard to claim 4, Rupley discloses the instruction buffer as claimed in claim 3, wherein the entries storing the instructions are lower in entry number than the entries storing no instructions. [Figure 5-7 show that once the instructions have progressed enough, there are entries at a higher entry number with no instructions compared to the entries at lower entry number with instructions.]

34. In regard to claim 6, Rupley discloses a method of controlling a buffer queue, comprising the steps of:

a. generating a first group of instructions in an order determined beforehand; [Figure 4 shows a buffer 20 for storing a group of 8 instructions. Column 6, lines 28-31 show that the instructions stored in the instruction buffer are stored in

program order (a preselected order). These instructions are inherently generated at some point in time.]

b. generating a second group of instructions belonging to said first group of instructions and capable of being executed; [The instructions ADD and BC_0 in entries 0 and 1 of the instruction buffer of figure 4 are a second group of instructions belonging to the first group (all 8 instructions) and capable of being executed (as shown in their dispatch in figures 5-10). These instructions are inherently generated as given above.]

c. and executing one of said second group of instructions highest in priority. [Figures 4-5 shows that the instruction at entry 0 is the first in order (a highest priority) and is dispatched to execution units and placed in the completion unit 24. Column 4, lines 25-34 show that when an instruction is dispatched for execution, it is placed in the completion buffer at the same time.]

35. In regard to claim 7, Rupley discloses the method as claimed in claim 6, further comprising the steps of:

a. generating a third group of instructions included in said first group of instructions; [The instructions MUL and BC_2 of entries 4 and 5 are a third group of instructions included in the first group of all 8 instructions.]

b. and generating a fourth group of instructions included in said first group of instructions and not dependent on said third group of instructions; [The instructions SUB and BC_1 of entries 2 and 3 are a fourth group of instructions included in the first group of instructions and that are not dependent on the fourth

group. Column 7, lines 35-39 show that instructions before BC_0 do not directly depend on the outcome of the branch. The same holds true for each branch and so the instructions of the fourth group are not dependent on the instructions, and specifically the branch (BC_2), of the third group since they are preceding in order.]

c. wherein when one of said fourth group of instructions highest in priority does not belong to said second group of instructions, none of said fourth group of instructions is executed. [The instruction of the fourth group that is highest in priority is the SUB instruction since it has a lower entry number and is closer to the front of the FIFO buffer. This instruction is not a part of the second group, which consists of the instructions in entries 0 and 1. A scenario is shown in figure 4 where this SUB instruction from the fourth group of instruction is highest in priority among the fourth group and does not belong to the second group of instructions and none of the instructions of the fourth group are executed at this time.]

36. In regard to claim 8, Rupley discloses the method as claimed in claim 7, wherein one of a preselected two instructions belonging to said third group or said fourth group is not executable until the other instruction is executed. [The two instructions of group four (BC_1 and MUL) are two preselected instructions. The progression from figures 5-6 shows that the SUB instruction is executed and placed in the completion unit before the BC_1 instruction is executed since it remains in the instruction buffer. Then in figure 7 it is shown that the BC_1 instruction is executed after the SUB instruction.]

37. In regard to claim 9, Rupley discloses the method as claimed in claim 8, wherein the instructions belonging to said third group are executed at the same time as the instructions belonging to said fourth group. [Figure 1 and column 4, lines 25-30 show that there are multiple functional units for executing instructions in parallel. Thus, when resources allow it, the instructions of groups three and four will execute in parallel.]

38. In regard to claim 10, Rupley discloses the method as claimed in claim 9, wherein the instructions belonging to said third group and the instructions belonging to said fourth group are operation instructions and memory access instructions respectively. [Figure 4 shows that the third group consists of MUL (multiply) and BC_2 (conditional branch) instructions. Since the conditional branch must resolve a condition it performs an operation and is an operation instruction just as the multiply instruction is. The fourth group of instructions consists of SUB (subtract) and BC_1 (conditional branch) instructions. It is inherent that a subtract instruction accesses either a main memory (or cache memory) or a register, which is a type of memory, in order to do the calculation. Therefore this instruction is a memory access instruction. A conditional branch instruction also must access some sort of memory to evaluate the condition, whether this memory is main memory, a general-purpose register, or a flag or status register.]

39. In regard to claim 11, Rupley discloses a buffer queue control comprising:

a. A reorder buffer for registering a plurality of instructions in an order of instructions; [Figures 2-9 show a reorder buffer or completion unit (element 24) that stores or registers a plurality of instructions in an order.]

b. A first buffer for storing first instructions included in the plurality of instructions; [Figures 2-9, element 20 is a first buffer that stores the plurality of instructions including first instructions, which the Examiner is taking to be the instructions at entries 0, 2, and 4, of figure 4 for example.]

c. A second buffer for storing, among the plurality of instructions, second instructions other than the first instructions; [Figures 2-9, elements 28a-28c are a second buffer that stores only the branch instructions of the plurality of instructions, which are different than the first instructions.]

d. Said second instructions including an instruction that should be issued after said first instructions; [As shown in figures 4-9 in the instruction buffer, the BC2 instruction should be executed after the first instructions since it is later in program order.]

e. Said first buffer including a plurality of first entries for sequentially storing the first instructions in said order of instructions; [Figure 4 shows that the first buffer sequentially (after or serially) stores the first instructions in said order.]

f. Said buffer queue control further comprising the steps of:

i. Releasing any one of the plurality of first entries that stores an instruction that is issued; [Figures 4-5 shows that the ADD instruction (among the first instruction and in one of the plurality of entries) is issued or dispatched and released from the first buffer.]

ii. Shifting any one of the first instructions that is not issued to an entry prior, in order, by one; [These figures then show that the next instruction among the first instructions (SUB) is shifted down, in order, one position.]

iii. Issuing one of the second instructions, which can be issued, earliest in said order of instructions; [As shown in figures 5-6, the BC0 instruction (one of the second) is issued earliest in the order at that time since it is at position 0 of the instruction buffer.]

iv. And deleting any one of the plurality of instructions that has been executed and is earlier, in said order of instructions, than instructions not executed. [As shown throughout figures 4-9, when an instruction is executed (and is before unexecuted instructions since it is at position 0) it is deleted from its position in the instruction buffer.]

40. In regard to claim 12, Rupley discloses the buffer queue control as claimed in claim 11 further comprising the step of issuing any one of the first instructions that is earliest in said order of instructions and ready to be issued. [As shown in figures 4-5, the ADD instruction (among the first instructions) is issued because it is earliest in said order and is ready to be issued since it is in entry 0.]

41. In regard to claim 13, Rupley discloses the buffer queue control as claimed in claim 12, wherein said second buffer comprises a plurality of second entries each for storing a particular one of the second instructions in said order of instructions, an issuance pointer for controlling issuance of said second instructions, and a head pointer indicative of an entry that has been issued last. [As shown above and in figures 4-9, the

second buffer has a plurality of entries for storing the second instructions in said order (which is the order they are placed in the buffer). Column 3, lines 34-52 illustrate that this buffer includes age bits for specifying what instructions in the buffer are earlier than the other instructions in the buffer and thus this age (head pointer) indicates which of the stored instructions in the second buffer was issued last. Column 3, lines 34-52 show that the second buffer controls branch misprediction resolution and thus also controls issuance of any second instructions in the first buffer that may be after the second instruction stored in the second buffer in program order and thus is or contains an issuance pointer.]

42. In regard to claim 14, Rupley discloses the buffer queue control as claimed in claim 13, wherein one of the first instructions can be executed at the same time as one of the second instructions. [As shown in figures 5-6, the BC0 (one of the second instructions) and SUB (one of the first instructions) instructions are dispatched at the same time and thus executed at the same time.]

43. In regard to claim 15, Rupley discloses the buffer queue control as claimed in claim 13, wherein the first instructions comprise operation instructions while the second instructions comprise memory access instructions. [As shown above, the first instructions are operation instructions such as ADD, SUB, and MUL and the second instructions are conditional branch instructions. It is inherent that the conditional branch instructions access some sort of memory, whether it be to check a flags register or check operands to compare and thus the branch instructions are memory access instructions.]

Response to Arguments

44. Applicant's arguments filed 10/05/04 have been fully considered but they are not persuasive.

45. Applicant has argued with regard to claim 1 that Rupley clearly does not answer the recitation of first and second buffers wherein each issues instructions in storage entry order. The Examiner notes, however, that claim 1 does not state that each of the first and second buffers issue instructions in storage entry order. The claim only states that the two buffers store instructions and that the second buffer stores instructions that are issued earlier before other instructions that are issued later. This does not necessitate that the second buffer issues the instructions.

46. Applicant has argued with respect to claim 2 that Rupley does not provide for each entry to indicate whether or not it is ready to be issued. Column 7, lines 59-67 show that the buffer is first-in-first-out (FIFO) in nature and after dispatch, or issue, of an instruction each instruction in the buffer decrements down into an entry with a lower entry number. Thus, as shown in figures 4-5, the instruction at entry 0 is ready to be issued. This is shown by the entries based on the entry number and if it is 0 or not.

47. Applicant has argued with respect to claim 3, that Rupley does not observe priority among instructions ready to be issued. First, claim 3 does not make any direct mention of priority, but the examiner is taking the type of priority the Applicant is referring to, to be priority associated with the lowest entry number. As shown above, instructions at slot 0 of the buffer are ready to be issued and inherently have the lowest entry number and are the next to be issued. Thus priority is observed.

48. Applicant has argued that Rupley does not provide priority among entries having instruction[s] to entries not having instructions. The Examiner assumes the Applicant is referring to claim 4 where it is mentioned that entries storing instruction are lower in entry number (higher in priority) than entries storing no instructions. Figure 5-7 show that once the instructions have progressed enough, there are entries at a higher entry number with no instructions compared to the entries at lower entry number with instructions and thus the entries with a higher priority are those with instructions.

49. Applicant argues that there is no teaching in Rupley concerning grouping of instructions with logical operations in regard to issuance of instructions in accordance with the group(s) to which a given instruction belongs as recited in claims 7 and 8. First, claims 7 and 8 make no mention of logical operations. Clearly as shown in figures 3-9 there are groups of instructions in the instruction buffer that are issued.

50. Applicant has argued that Rupley does not differentiate between groups of memory access and operation instructions as in claim 10. The claims do not state the requirement of differentiating between groups of memory access and operational instructions but instead gives simple circumstance where the third group are composed of operational instructions and the fourth of memory access instructions. Figure 4 shows that the third group consists of MUL (multiply) and BC_2 (conditional branch) instructions. Since the conditional branch must resolve a condition it performs an operation and is an operation instruction just as the multiply instruction is. The fourth group of instructions consists of SUB (subtract) and BC_1 (conditional branch) instructions. It is inherent that a subtract instruction accesses either a main memory (or

cache memory) or a register, which is a type of memory, in order to do the calculation. Therefore this instruction is a memory access instruction. A conditional branch instruction also must access some sort of memory to evaluate the condition, whether this memory is main memory, a general-purpose register, or a flag or status register.

Conclusion

51. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

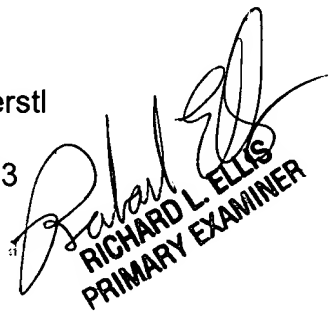
52. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183



SFG
December 21, 2004